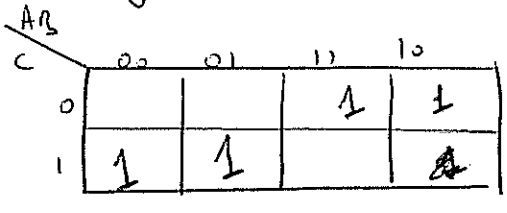
Solving Session 5 EECE320

A	B	C	3x+3 in decimal	X5	X4	X3	X2	X1
0	0	0	3	0	0	0	1	1
0	0	1	6	0	0	1	1	0
0	1	0	9	0	1	0	0	1
0	1	1	12	0	1	1	0	0
1	0	0	15	0	1	1	1	1
1	0	1	18	1	0	0	1	0
1	1	0	21	1	0	1	0	1
1	1	1	24	1	1	0	0	0

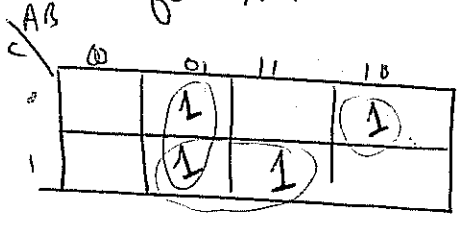
$X_1 = C'$

$X_2 = B'$

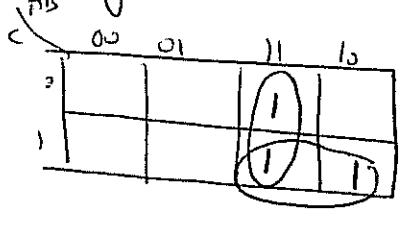
for X_3:



for X_4:



for X_5:



$X_3 = A'C + AC'$

$X_4 = A'B + BC + AB'C'$

$X_5 = AB + AC$

```
library ieee
use ieee.std_logic_1164.all;

entity circuit is
  port ( A, B, C : in std_logic;
         X : out std_logic_vector (4 downto 0));
end circuit;

architecture fff of circuit is

  function AA ( A, B, C : std_logic ) return std_logic_vector (4 downto 0) is
  X : std_logic_vector (4 downto 0);
  begin
    ① if C = '0'
        then X(0) <= 1
      else X(0) <= 0
      end if;
    ② if B = '0'
        then X(1) <= 1
      else X(1) <= 0
      end if;
    ③ if (A = 0 and C = 1) or (A = 1 and C = 0)
        then X(2) <= 1
      else X(2) <= 0.
      end if
    ④ if (A = 0 and B = 1) or (B = 1 and C = 1) or (A = 1 and B = 0
                                                    and C = 0)
        then X(3) = 1
      else X(3) <= 0 ; end if;
    ⑤ if (A = 1 and B = 1) or (A = 1 and C = 1)
        then X(4) <= 1
      else X(4) <= 0) ; end if;
```

(I)

```
    return X;
end AA;
begin
    X <= AA(A, B, C);
end fff;
```

---

architecture dataflow of circuit is ——— (II)

```
begin
    X(0) <= Nor C;
    X(1) <= Nor B;
    X(2) <= ((Nor A) and C) OR (A and (Nor C));
    X(3) <= ((Nor A) and B) or (B and C) or (A and (Nor B) and Nor C));
    X(4) <= (A and B) OR (A and C).;
end dataflow;
```

---

architecture behavioral of circuit is ——— (III)

```
begin
    procss (A, B, C)
        begin
```

(1) (2) (3) (4) (5) → from the function description

```
    end process;
```

Test bench

```
entity test is
end test;
architecture test of test is
  component Circuit
    port (A,B,C : in std_logic;
          X : out std_logic_vector (4 downto 0));
  end component
  signal A,B,C : std_logic
  signal X : std_logic_vector (4 downto 0);

U1 : circuit port map (A,B,C,X);
process
begin
  A<=0 ; B<=0 ; C<=0 wait for 10 ns
  :
  :
wait;
end process;
end test.
```